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Date of Filing	:	25 JUNE 2002
Application Number	:	200203823-0
Applicant(s)	:	AGILENT TECHNOLOGIES, INC.
Title of Invention	:	ERROR DETECTOR WITH CORRECTION CIRCUIT

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PATENTS FORM 1
Patents Act
(Cap. 221)
Patents Rules
Rule 19

ACTION

INTELLECTUAL PROPERTY OFFICE OF SINGAPORE

101101

REQUEST FOR THE GRANT OF A PATENT UNDER SECTION 25

* denotes mandatory fields

1. YOUR REFERENCE* 70010721-1

2. TITLE OF INVENTION* Error Detector With Correction Circuit

3. DETAILS OF APPLICANT(S)* (see note 3) Number of applicant(s): 01

(A) Name: Agilent Technologies, Inc.

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[X] For corporate applicant [] For individual applicant

State of incorporation: Delaware State of residency: California

Country of incorporation: USA Country of residency: USA

[] For others (please specify in the box provided below)

(B) Name:

Address:

State: Country:

NS-OK 27/6/

25 JUN 2002
200203823-0

☐ For corporate applicant ☐ For individual applicant

State of incorporation | State of residency

Country of incorporation | Country of residency

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(C) Name

Address

State | Country

☐ For corporate applicant ☐ For individual applicant

State of incorporation | State of residency

Country of incorporation | Country of residency

☐ For others (please specify in the box provided below)

☐ Further applicants are to be indicated on continuation sheet 1

4. DECLARATION OF PRIORITY (see note 5)

A. Country/country designated

File number | Filing Date DD MM YYYY

B. Country/country designated

File number | Filing Date DD MM YYYY

☐ Further details are to be indicated on continuation sheet 6

5. INVENTOR(S)* (see note 6)

A. The applicant(s) is/are the sole/joint inventor(s) Yes ☐ No ☒

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B. A statement on Patents Form 8 is/will be furnished Yes [X] No []

6. CLAIMING AN EARLIER FILING DATE UNDER (see note 7)

[] section 20(3) [] section 26(6) [] section 47(4)

Patent application number

DD MM YYYY

Filing Date

Please mark with a cross in the relevant checkbox provided below
(Note: Only one checkbox may be crossed.)

[] Proceedings under rule 27(1)(a)

DD MM YYYY

Date on which the earlier application was amended

[] Proceedings under rule 27(1)(b)

7. SECTION 14(4)(C) REQUIREMENTS (see note 8)

Invention has been displayed at an international exhibition. Yes [] No [X]

8. SECTION 114 REQUIREMENTS (see note 9)

The invention relates to and/or used a micro-organism deposited for the purposes of disclosure in accordance with section 114 with a depository authority under the Budapest Treaty.

Yes [] No [X]

9. CHECKLIST*

(A) The application consists of the following number of sheets

i.	Request	05	Sheets
ii.	Description	18	Sheets
iii.	Claim(s)	6	Sheets
iv.	Drawing(s)	7	Sheets
v.	Abstract (Note: The figure of the drawing, if any, should accompany the abstract)	1	Sheets
Total number of sheets		37	Sheets

(B) The application as filed is accompanied by:

[] Priority document(s) [] Translation of priority document(s)

25 JUN 2002
20020823-0

[X] Statement of inventorship & right to grant

[] International exhibition certificate

10. DETAILS OF AGENT (see notes 10, 11 and 12)

Name

Firm: Agilent Technologies Singapore (Sales) Pte Ltd

11. ADDRESS FOR SERVICE IN SINGAPORE* (see note 10)

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Building Name: Alexandra Point

Postal Code: 119958

12. NAME, SIGNATURE AND DECLARATION (WHERE APPROPRIATE) OF APPLICANT OR AGENT* (see note 12)
(Note: Please cross the box below where appropriate.)

[X] I, the undersigned, do hereby declare that I have been duly authorised to act as representative, for the purposes of this application, on behalf of the applicant(s) named in paragraph 3 herein.

JAMES SEYMOUR

Name and Signature

DD MM YYYY: 24/06/2002

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NOTES:

1. This form when completed, should be brought or sent to the Registry of Patents together with the rest of the application. Please note that the filing fee should be furnished within the period prescribed.

2. The relevant checkboxes as indicated in bold should be marked with a cross where applicable.

3. Enter the name and address of each applicant in the spaces provided in paragraph 3.
 Where the applicant is an individual
 - Names of individuals should be indicated in full and the surname or family name should be underlined.
 -The address of each individual should also be furnished in the space provided.
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 Where the applicant is a body corporate
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 - The address of the body corporate should also be furnished in the space provided.
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 Where the applicant is a partnership
 - The details of all partners must be provided. The name of each partner should be indicated in full and the surname or family name should be underlined.
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6. Where the applicant or applicants is/are the sole inventor or the joint inventors, paragraph 5 should be completed by marking with a cross the 'YES' checkbox in the declaration (A) and the 'NO' checkbox in the alternative statement (B). Where this is not the case, the 'NO' checkbox in declaration (A) should be marked with a cross and a statement will be required to be filed on Patents Form 8.

7. When an application is made by virtue of section 20(3), 26(6) or 47(4), the appropriate section should be identified in paragraph 6 and the number of the earlier application or any patent granted thereon identified. Applicants proceeding under section 26(6) should identify which provision in rule 27 they are proceeding under. If the applicants are proceeding under rule 27(1)(a), they should also indicate the date on which the earlier application was amended.

8. Where the applicant wishes an earlier disclosure of the invention by him at an International Exhibition to be disregarded in accordance with section 14(4)(c), then the 'YES' checkbox at paragraph 7 should be marked with a cross. Otherwise, the 'NO' checkbox should be marked with a cross.

9. Where in disclosing the invention the application refers to one or more micro-organisms deposited with a depository authority under the Budapest Treaty, then the 'YES' checkbox at paragraph 8 should be marked with a cross. Otherwise, the 'NO' checkbox should be marked with a cross. Attention is also drawn to the Fourth Schedule of the Patents Rules.

10. Where an agent is appointed, the fields for "DETAILS OF AGENT" and "ADDRESS FOR SERVICE IN SINGAPORE" should be completed and they should be the same as those found in the corresponding Patents Form 41. In the event where no agent is appointed, the field for "ADDRESS FOR SERVICE IN SINGAPORE" should be completed, leaving the field for "DETAILS OF AGENT" blank.

11. In the event where an individual is appointed as an agent, the sub-field "Name" under "DETAILS OF AGENT" must be completed by entering the full name of the individual. The sub-field "Firm" may be left blank. In the event where a partnership/body corporate is appointed as an agent, the sub-field "Firm" under "DETAILS OF AGENT" must be completed by entering the name of the partnership/body corporate. The sub-field "Name" may be left blank.

12. Attention is drawn to sections 104 and 105 of the Patents Act, rules 90 and 105 of the Patents Rules, and the Patents (Patent Agents) Rules 2001.

13. Applicants resident in Singapore are reminded that if the Registry of Patents considers that an application contains information the publication of which might be prejudicial to the defence of Singapore or the safety of the public, it may prohibit or restrict its publication or communication. Any person resident in Singapore and wishing to apply for patent protection in other countries must first obtain permission from the Singapore Registry of Patents unless they have already applied for a patent for the same invention in Singapore. In the latter case, no application should be made overseas until at least 2 months after the application has been filed in Singapore, and unless no directions had been issued under section 33 by the Registrar or such directions have been revoked. Attention is drawn to sections 33 and 34 of the Patents Act.

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Error Detector With Correction Circuit

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This invention relates to a method and apparatus for detecting errors in pseudo-random bit sequences.

Background

In recent years, the performance of communication systems has reached a level where serial data is routinely sent at transmission rates in excess of 2.5 gigabits per second. To achieve these transmission rates, the signal-to-noise ratio of communication equipment is often lowered to a level where errors become significant.

Typically, communication equipment is designed to have a bit error rate which is lower than the maximum tolerated bit error rate of a communication system in which the communication equipment operates. For example, physical layer specifications for the Asynchronous Transfer Mode (ATM) protocol allow a maximum bit error rate of 10^{-10}. Accordingly, the bit error rate of communication equipment is often measured both in production and in-situ to determine if the rates conform with system specifications.

Pseudo-random bit sequences (PRBS) are commonly used in Bit Error Rate (BER) measurements, and devices which perform these measurements are often referred to as Bit Error Rate Testers (BERTs).

Figure 1 illustrates the basic features of a communication system incorporating PRBS error measurement. The communication system 100 comprises a transmitter 110 coupled to an input of a communication channel 120 for transmitting a signal over the communication channel, and a receiver 130 coupled to an output of the communication channel 120 for receiving the signal transmitted over the communication channel 120.

PRBS error measurement is implemented in the communication system 100 using two main components: a PRBS generator 140 and a PRBS error detector 150. The PRBS generator 140 creates a signal containing PRBS data. This signal is provided to the transmitter 110, which transmits the signal over the communication channel 120. The receiver 130 receives the transmitted signal containing the PRBS data created by the PRBS generator, and passes the PRBS data to the PRBS error detector 150. The PRBS error detector 150 counts the number of bit errors in the PRBS data over time to determine a bit error rate.

In some systems, the signal from the PRBS generator is a baseband signal, and the transmitter 110 up-converts the baseband signal into a higher frequency transmission signal suitable for transmission over the communication channel 120. The receiver 130 then receives the transmission signal and down-converts the signal back to a baseband signal to recreate the PRBS data.

In other systems, the signal from the PRBS generator is provided at a frequency suitable for transmission over the communication channel 120. In such systems, there is no up-conversion of the signal at the transmitter, and no down-conversion of the signal at the receiver.

Reasons for using a PRBS include:

(1) The PRBS has the same statistical characteristics as a truly random bit sequence, i.e., on average there are an equal number of zero value bits as one value bits. When testing communication equipment for bit errors, a truly random sequence is generally a good model for real data.

(2) The PRBS is an algorithmically deterministic bit sequence, which means that the next bit in the sequence depends only on the state of the system generating the bit sequence, i.e., it is completely predictable. The PRBS error detector 150 uses this characteristic of the PRBS to predict the next bit in the received PRBS. Any discrepancy between the predicted next bit and the actual next bit received is detected as a bit sequence error in the PRBS error detector 150.

PRBS generators and PRBS error detectors are known, for example, from US patent number 6,002,714. As shown in Figure 2, this patent describes in detail the operation of a PRBS generator 140 comprising a 7-stage shift register 141, 142, 143, 144, 145, 146, 147 tapped at the output of the 6th and 7th registers 146, 147. The patent also describes in detail the operation of a PRBS error detector 150 which comprises a complementary 7-stage shift register 151, 152, 153, 154, 155, 156, 157 tapped at the output of the 6th and 7th registers 156, 157, as shown in Figure 3.

Since the PRBS generator 140 and PRBS error detector 150 have been described in detail in US 6,002,714, no further details will be given here except to say that the generator 140 outputs a cyclical PRBS of length $2^7 - 1$.

Referring to Figures 2 and 3, the PRBS error detector 150 receives at an input 160 the transmitted PRBS output 165 of the PRBS generator 140. If seven sequential bits have been output by the PRBS generator 140, then the next bit output from the PRBS generator 140 will be the result of an XOR operation on the first two bits. Assuming that the seven sequential bits from the PRBS generator are then received via the input 160 of the PRBS error detector 150 without error, then the state of the 7-stage shift register in the PRBS error detector 150 will be identical to the state of the 7-stage shift register in the PRBS generator 140 just before the next bit is generated. To predict the next bit generated by the PRBS generator 140, the PRBS error detector 150 comprises an XOR logic gate 158 which

performs an XOR operation on the first two received bits of the seven sequential bits from the PRBS generator. Because the PRBS error detector 150 taps the shift register at the same points as the PRBS generator 140, the XOR gate 158 outputs a predicted next bit, which is a prediction of the next bit that will be received from the PRBS generator 140 . A further XOR logic gate 159 performs a comparison between the predicted next bit output by the XOR gate 158, and the received next bit, which is the next bit received at the input 160 of the PRBS error detector 150.

If there is no error during the transmission of the next bit from the PRBS generator 140 then the predicted next bit will be the same value as the received next bit. In this case, the XOR gate 159 will generate a zero-value output indicating no error. Conversely, if there is an error during the transmission of the next bit from the PRBS generator then the received next bit will differ from the predicted next bit. In this case, the XOR gate 159 will detect the difference and will generate an output indicating an error, in this case a logic high output.

In operation, the PRBS error detector receives a portion of the PRBS into a 7-stage shift register 151, 152, 153, 154, 155, 156, 157 and taps the register to generate a predicted next bit at the output of an XOR logic gate 158. A second XOR logic gate 159 receives a next bit of the PRBS and compares this received next bit with the predicted next bit. The output 170 of the second XOR gate 159 then indicates whether there is a difference between the received next bit and the predicted next bit and thus whether there is an error in the received PRBS. The PRBS detector operates on subsequent bits of the PRBS in the same manner.

A drawback with the PRBS error detector 150 is that it assumes the portion of the PRBS stored in the 7-stage shift register contains no errors. If an error exists in any of the bits stored in the shift register then the PRBS error detector 150 will generate an erroneous predicted next bit when the erroneous bit reaches both stages 6 and 7 of the shift register. The erroneous predicted next bit will cause the second XOR gate 159 to generate an error

signal at the output of the second XOR gate 159 when the received next bit is correct, or to generate no error signal when the received next bit is erroneous.

When an erroneous bit is received in the PRBS error detector 150, the second XOR gate 159 will output an error signal as described above. However, that erroneous bit also enters the 7-stage shift register, propagating through the register, and causing erroneous prediction of the predicted bit when the error bit is tapped from the 6th and 7th shift registers 156, 157. Assuming there are no further received error bits, then the two erroneous predictions of the predicted bit cause the second XOR gate 159 to generate two further error signals. Thus, for each error bit received in isolation, the PRBS error detector will generate 3 error signals.

For the PRBS error detector 150, the bit error rate may be calculated by dividing the number of error signals received during an observation period by the length of the observation period, and then dividing that result by a factor of three to account for the three error signals generated for each received error bit. However, this calculation assumes that the error bits are received in isolation i.e., no more than one error bit is received every 7 cycles. If error bits are received more frequently than once every 7 bits then there will not necessarily be 3 error signals produced for each received error bit, and in general fewer than three error signals will be generated. For example, two consecutive error bits received in the PRBS error detector 150 will produce only 4 error signals, 2 error signals fewer than if the error bits had been received separately.

The problem of non-isolated error bits in PRBS error detectors can either be ignored as a statistically unlikely event, or solved using statistical analysis to determine the likely number of these non-isolated error bits, and re-factor the bit error rate based on the analysis. Both of these approaches assume a statistical model for distribution of error bits. Statistical models only provide best estimates for the distribution of error bits, and it is therefore inevitable that the bit error rate measured using these approaches will not be completely accurate. For

example, if the statistical model assumes a random distribution of error bits then error bits resulting from systematic errors in the communication channel will potentially be ignored. A further drawback with the statistical analysis approach is that it requires additional computation which adds to the complexity, reliability and cost of a bit error rate tester.

Summary Of The Invention

According to the present invention there is provided a detector for detecting errors in a pseudo-random bit sequence (PRBS), and a method of detecting an error in a pseudo-random bit sequence (PRBS).

According to a first aspect of the invention, the detector comprises a correction circuit which is a responsive to the output signal indicating an error in the received next bit for correcting the error in the received next bit. The detector may also comprises a predictor configured to receive a portion of the PRBS and predict a next bit of the PRBS based on the received portion, and a comparator configured to receive the next bit of the PRBS, compare the received next bit with the predicted next bit to detect if there is an error in the received next bit, and output a signal indicative of an error in the received next bit.

A detector in accordance with the first aspect of the present invention has the advantage that by correcting the error in the received next bit, the detector is able to prevent errors in future predictions of received next bits.

In a preferred embodiment of the invention, the predictor comprises a linear series of shift registers. The predictor may further comprise a tapping circuit coupled to the output of at least two of the shift registers.

Suitably, the correction circuit of the detector is coupled to the predictor for correcting the error in the received next bit as it propagates through the predictor. Preferably, the correction circuit corrects the error in the received next bit before it is output to any portion of the tapping circuit.

The correction circuit may be coupled to the linear series of shift registers to correct the error in the received next bit as it propagates through the shift registers, preferably as the received next bit propagates from the output of one shift register and the input of a next consecutive shift register.

According to a second aspect of the present invention there is provided a method of detecting an error in a pseudo-random bit sequence (PRBS), and upon detecting an error, correcting the received next bit in the PRBS. Preferably, the method further comprises receiving the PRBS, predicting a next bit of the PRBS based on a received portion of the PRBS; comparing the received next bit with the predicted next bit to detect if there is an error in the received next bit.

Preferably, the method further comprises predicting another next bit of the PRBS based on a portion of the PRBS including the corrected received next bit.

Figures

Embodiments of the invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a schematic diagram illustrating the basic features of a communication system incorporating PRBS error measurement;

Figure 2 is a schematic diagram of a PRBS generator according to the prior art;

Figure 3 is a schematic diagram of a PRBS error detector according to the prior art;

Figure 4 is a schematic diagram of a PRBS error detector in accordance with the present invention;

Figure 5 is a schematic diagram of a trigger circuit for use in the PRBS error detector shown in Figure 4;

Figure 6 is a schematic diagram of a PRBS error detector in accordance with the present invention including a trigger circuit; and

Figure 7 is a flow chart showing the operating states of the trigger circuit of Figure 6.

Detailed Description

Referring to Figure 4, there is shown a PRBS detector 400 in accordance with the present invention. The PRBS detector 400 comprises 3 main functional elements: 1) a predictor 430, 2) a comparator 440, and 3) a correction circuit 450.

Predictor

The predictor 430 includes an input 434 for receiving the PRBS under test, a linear series shift register, and a tapping circuit.

The linear series shift register comprises 23 individual shift registers 401, 402, 403, 404, 418, 419, and 423. Shift registers 5-17 and 20-22 are represented in Figure 4 by a series of 3 dots for the sake of clarity. Each shift register comprises an input and an output, with the output of the first shift register 401 being coupled to the input of the second shift register 402, and the output of the second shift register 402 being coupled to the input of the third shift register 403, and so on until the input of the twenty-third shift register 423.

The tapping circuit comprises two tapping lines 425, 436 and a first XOR gate 427. A first tapping line 425 taps the output of the eighteenth shift register 418, while a second tapping line 426 taps the output of the twenty-third shift register 423. The two tapping lines 425, 426 are coupled to the two inputs of the XOR gate 427.

The function of the predictor 430 is to receive a portion of a PRBS, and predict a next bit of the PRBS based on the received portion. The predictor 430 has been designed to predict a next bit in a PRBS signal generated by a PRBS generator having an equivalent number of shift registers (23 shift registers) and equivalent tapping points (taps 18 and 23). Such as PRBS signal would have a pattern count equal to $2^{23} - 1$.

The predicted next bit is provided at the output of the first XOR gate 427.

Comparator

The function of the comparator 440 is to receive the next bit of the PRBS, compare the received next bit with the predicted next bit to detect if there is an error in the received next bit, and output a signal indicative of an error in the received next bit. To achieve this function, the comparator 440 of the present embodiment comprises a re-timing shift register 422, two supply lines 424, 436, and a second XOR gate 428.

The predicted next bit is provided from the first XOR gate 427 to a first input of the second XOR gate 428 via the re-timing shift register 422. The re-timing shift register 422 is included to prevent setup time violations which can occur when one logic gate is connected directly to another logic gate. To achieve the higher bit rates, the present design provides for one level combination logic only in between shift registers. Instead of feeding the output of the first XOR gate 427 to the input of the second XOR gate 428, the re-timing shift register 422 is added to ensure accurate data and no setup time violation. To compensate for the one cycle delay in the comparator 440, the supply line 426 supplies the received next bit from the output of the first shift register 401 to a second input of the second XOR gate 428.

The supply line 424 supplies the predicted next bit from the output of the re-timing shift register 422 to a second input of the second XOR gate 428. The second XOR gate 428 performs an XOR operation on the received next bit and the predicted next bit such that the gate outputs a high logic signal only when there is a difference between the logic values of the received next bit and the predicted next bit. If the logic values of the received next bit and the predicted next bit match then the second XOR gate 428 outputs a zero signal. A difference between the logic value of the received next bit and the logic value of the

predicted next bit indicates that there is an error in the received next bit. Consequently, a high logic signal output by the second XOR gate 428 is indicative of an error in the received next bit.

In operation, the PRBS error detector 400 receives a portion of the PRBS into the 23-stage shift register and taps the register to generate a predicted next bit at the output of the XOR gate 427. A second XOR logic gate 428 receives a next bit of the PRBS and compares this received next bit with the predicted next bit. The output of the second XOR gate 428 then indicates whether there is a difference between the received next bit and the predicted next bit and thus whether there is an error in the received PRBS. The PRBS detector operates on subsequent bits of the PRBS in the same manner.

A drawback with prior art PRBS error detectors, such as the detector shown in Figure 3, is that they assume the portion of the PRBS stored in the linear series shift register contains no errors. If an error exists in any of the bits stored in the linear series shift register then the PRBS error detector will generate an erroneous predicted next bit when the erroneous bit reaches the tapped stages of the linear series shift register. The erroneous predicted next bit will cause the comparator stage of the PRBS error detector to generate an error signal when the received next bit is correct, or to generate no error signal when the received next bit is erroneous.

Correction Circuit

To account for received error bits entering the linear series shift register of the predictor 430, the PRBS error detector 400 according to the invention further comprises a correction circuit 450.

The correction circuit 450 operates in response to the output signal of the second XOR gate 428. When the output signal indicates an error in the received next bit then the correction circuit 450 corrects the error by changing the value of the received next bit as it propagates through the linear series shift register.

According to a first embodiment shown in Figure 4, the correction circuit 450 comprises a feedback line 452 coupled to the output of the second XOR gate 428, two re-timing shift registers 454, 456, an AND gate 458, a trigger circuit 460, and a third XOR gate 462.

The feedback line 452 supplies the output signal as a correction signal from the second XOR gate 428 via the first re-timing shift register 454 to a first input of the AND gate 458. Meanwhile, the trigger circuit 460 supplies a trigger signal to a second input of the AND gate 458. The output of the AND gate 458 is supplied via the second re-timing shift register to a first input of the third XOR gate 462.

The AND gate 458 provides a switch for switching on and off the correction circuit 450. The switching operation of the AND gate 458 is controlled by the trigger signal from the trigger circuit 460. When the trigger circuit 460 supplies a logic-zero signal to AND gate 458, the output of the AND gate 458 is always zero regardless of the value of the correction signal supplied by the feedback line 452. However, when the trigger circuit 460 supplies a logic-high signal to AND gate 458, the AND gate 458 outputs a signal corresponding to the first input. Consequently, the correction signal supplied by the feedback line 452 to the first input passes unaltered through the AND gate 458.

The third XOR gate 462 is positioned in-between the third and fourth shift registers of the predictor 430. Specifically, the output of the third shift register 403 couples to the second input of the third XOR gate 462, and the output of the third XOR gate 462 couples to the input of the fourth shift register 404. The position of the third XOR gate 462 enables the

values in the linear series shift register to be altered by the correction circuit to correct erroneous bits which enter the linear series shift register from the input 434.

When the first input to the third XOR gate 462 is set to logic-zero, the value of the output of the third XOR gate 462 is equal to the value of the second input to the third XOR gate 462. Hence, the output of the third shift register 403 is passed unaltered to the input of the fourth shift register 404.

However, when the first input to the third XOR gate 462 is set to logic-high, the value of the output of the third XOR gate 462 is equal to the inverted value of the second input to the third XOR gate 462. Hence, the value of the received bit stored in the third shift register 403 is inverted as it propagates from the output of the third shift register 403 to the input of the fourth shift register 404.

The purpose of the re-timing shift registers 454, 456 is to ensure that the correction signal is accurate and free from setup time violations as it passes through the correction circuit 450. The operation of the correction circuit 450 will now be described assuming that the trigger circuit 460 has switched on the correction circuit.

When no error bits are received by the detector 400, the second XOR gate 428 outputs a constant zero output signal, indicating that there are no errors in the PRBS. The constant zero output signal is tapped by the feedback line 452 to form a constant zero correction signal in the correction circuit 450. The correction circuit 450 supplies the constant zero correction signal to the third XOR gate 462, resulting in the output of the third shift register 403 passing unaltered to the input of the fourth shift register 404. Therefore, when there are no error bit received by the detector 400, the correction circuit performs no corrections as expected.

When an erroneous bit in a PRBS is received by the detector, it is stored for one clock cycle in the first shift register 401. At the end of the first clock cycle, the erroneous bit is output to the second shift register 402. At the same time, the erroneous bit is tapped by the comparator 440, which detects the error in the received bit, and generates a logic-high output signal from the output of the second XOR gate 428. The logic-high output signal is tapped by the feedback line 452 to form a logic-high correction signal in the first re-timing shift register 454 of the correction circuit 450.

At the end of the second clock cycle, the erroneous bit is output to the third shift register 403, and simultaneously, the logic-high correction signal is output from the first re-timing shift register 454 via the AND gate 458 to the second re-timing shift register 456.

At the end of the third clock cycle, the erroneous bit is output from the third shift register 403 to the second input of the third XOR gate 462, and simultaneously, the logic-high correction signal is output from the second re-timing shift register 456 to the first input of the third XOR gate 462. The logic-high correction signal causes the third XOR gate 462 to invert the erroneous bit and output a corrected received bit to the fourth register 404. Eventually, the corrected received bit propagates to the tapped 18th and 23rd shift registers to provide a correct prediction of a future received bit.

Trigger Circuit

It is preferable to switch on the correction circuit 450 using the trigger circuit 460 only when the detector 450 is operating in a stable state. The stable state can be determined through observation of the output signal from the second XOR gate 428 whereby the trigger circuit can be activated manually once the determination has been made. It is also possible for the trigger circuit to be activated by a simple timer.

Preferably, the trigger circuit is activated through active feedback monitoring of the output signal from the second XOR gate 428 as indicated by the optional feedback line 464 in Figure 4.

Figure 5 illustrates a trigger circuit 500 of the type suitable for use in the detector 400 of Figure 4.

The trigger circuit 500 makes sure that no error is residing in the linear series shift register before switching on the correction circuit. The trigger circuit 500 operates on the principle of counting a suitable number of consecutive logic-zeros output by the second XOR gate 428.

The trigger circuit 500 includes an input IN which is coupled to a series of shift registers 501-507. Initially, all the shift registers 501-507 are reset to logic "1" and the input IN is supplied with a continuous logic-high signal to maintain the logic "1" values.

When the trigger circuit is enabled, the input IN then receives the output signal of the second XOR gate 428 via the feedback line 464. The output signal passes into the series of shift registers. If there are no errors then a logical "0" signal representing no errors will propagate into this shift register series until it reach the last shift register 507. The logical "0" output of the last shift register is inverted to a logical "1" signal by an inverter 508. The logical "1" signal passes from the inverter 508 into a hold circuit 509, which to holds the logical "1" signal regardless of what signals are subsequently output by the inverter 508. The output signal from the hold circuit 509 provides the trigger signal to the AND gate 458 shown in Figure 4.

If a logical "1" signal, representing an error in the PRBS, enters the input IN before all the shift registers fill up with logical "0"s; a series of OR gates 511-516 will reset the shift registers 502-507 to logical "1". The trigger circuit must then recount the number of

consecutive logical "0" again by propagating logical "0" into the shift registers. The number of consecutive logical "0"s counted by the trigger circuit depends on the number of shift registers. Accordingly, a desired count can be achieved by an appropriate number of shift registers. In the trigger circuit 500, there are 7 shift registers making the count suitable for a predictor with 7 shift registers, i.e., for a 2^7 -1 PRBS detector circuit. A trigger circuit suitable for the predictor of Figure 4 would have at least 23 shift registers.

Figures 6 illustrates an alternative trigger circuit 650 with a modified correction circuit containing additional delay shift registers 690. Figure 7 is a flow chart illustrating the state of low speed block during operation. The trigger circuit 650 improves on the trigger circuit 500 by placing less load on input signal 664 received from the XOR gate 628. The input signal 664 drives an input of one OR gate rather than the numerous OR gates of the trigger circuit 500.

The purpose of this trigger circuit 650 is the same as the trigger circuit 500 of Figure 5, which is to switch on the correction circuit at a time when the predictor circuit is free of PRBS error bits. The trigger circuit 650 comprises two hold circuits (Circuit 2 and Circuit 3), one "RISING EDGE CHECKER" circuit, one low speed state machine 655, and three shift registers 661, 662, 663. Initially, the shift registers 662, 663 are reset to logical "0", and the shift register 661 of Circuit 1 is reset to logical "0" as well by low speed circuit 655. According to the state diagram, when "StartErrorCounting" equals logical "0", "Enable" and "NReset" will be equal to logical "0"; these will force all the shift registers of circuit 1, 2 and 3 equal to logical "0". Once "StartErrorCounting" is changed to logical "1", "NReset" will be asserted to logical "1", this will make the shift register 661 of Circuit 1 live (by setting the shift register 661 to zero). The shift register 661 will change to logical "1" if any error signal occurs from the PRBS Error Checker.

A low speed counter inside the low speed state machine 655 will start counting for a time period equal or greater than 7.36 ns (320 ps X 23). 320 ps is the period of the pattern running at, in this case, 3.125 GHz. 23 is the length of the pattern, in this case, 2^23 – 1. For a low speed counter running at 200 MHz, it will count to two, which is 10 ns (5 ns x 2). Once it completes the counting, Enable signal will be activated. If "Enable" is asserted earlier than Circuit 1, flip-flop of Circuit 2 will be asserted to logical "1", this logical "1" will propagate to circuit 3 and will be held at logical "1" regardless of the subsequent input signal. Output of Circuit 3 will be used as a trigger signal for the correction circuit AND gate 658.

If an error is detected in the PRBS before the low speed counter completes the counting then the "Enable" signal from low speed counter will be asserted later than error signal from Circuit 1. Circuit 2 will stay at logical "0" regardless of the subsequent signal from the low speed counter, since the logical "1" signal will not change due to the "HOLD" Circuit 1. An indication from "EnableIndicator" signal informs the low speed counter 655 that the trigger signal has not been activated successfully. The state machine 655 will then reset the shift register of Circuit 1 to zero and reactivate the trigger circuit feature again by rerunning the whole process of counting and enabling.

The additional four delay shift registers 690 compensate for the number of cycles that have been used by Circuit 1, 2 and 3.

Advantages of the trigger circuit of Figure 6 are that every gate has no more than 2 fanouts which is important in reducing the loading of the circuit for high speed applications. The number of shift registers will not increase with the increase of the pattern length. Low speed state machine can be synthesized with a standard library cell.

It will be evident in view of the foregoing description that various modifications may be made within the scope of the present invention. For example there may be more or less than 23 shift registers in the predictor.

CLAIMS

1. A detector for detecting errors in a pseudo-random bit sequence (PRBS), comprising:

a predictor configured to receive a portion of the PRBS, and predict a next bit of the PRBS based on the received portion,

a comparator configured to receive the next bit of the PRBS, compare the received next bit with the predicted next bit to detect if there is an error in the received next bit, and output a signal indicative of an error in the received next bit, and

a correction circuit responsive to the output signal indicating an error in the received next bit for correcting the error in the received next bit.

2. A detector as claimed in claim 1, wherein the correction circuit is coupled to the predictor for correcting the error in the received next bit as the received next bit propagates through the predictor.

3. A detector as claimed in claim 2, wherein the predictor is configured to predict a subsequent next bit of the PRBS based on a received portion of the PRBS that includes the received next bit corrected by the correction circuit.

4. A detector as claimed in claim 1, wherein the predictor comprises a linear series of shift registers, and a tapping circuit coupled to the output of two of the shift registers.

5. A detector as claimed in claim 4, wherein the tapping circuit is coupled to the output of the last shift register.

6. A detector as claimed in claim 4, wherein the tapping circuit further comprises an exclusive OR gate configured to receive the tapped output of two of the shift registers, and output the predicted next bit.

7. A detector as claimed in claim 4, wherein the correction circuit is coupled to the linear series of shift registers for correcting the error in the received next bit as the received next bit propagates through the shift registers.

8. A detector as claimed in claim 4, wherein the correction circuit is coupled to the output of a first shift register and the input of a second consecutive shift register for correcting the error in the received next bit as the received next bit propagates from the first to the second shift register.

9. A detector as claimed in claim 8, wherein the correction circuit comprises an exclusive OR gate configured to receive both the output of the first shift register and the output signal of the comparator, and output a corrected signal to the input of the second bit shift register.

10. A detector as claimed in claim 1, wherein the correction circuit is coupled to the comparator to receive the output signal.

11. A detector as claimed in claim 1, wherein the comparator detects if there is an error in the received next bit by detecting a difference between the predicted next bit and the received next bit.

12. A detector as claimed in claim 1, wherein the comparator comprises an exclusive OR gate configured to receive both the next bit of the PRBS and the predicted next bit.

13. A detector as claimed in claim 1, further comprising a switch circuit for monitoring the output signal of the comparator over a predetermined period, and for switching on the correction circuit when the output signal indicates no error during the predetermined period.

14. A method of detecting an error in a pseudo-random bit sequence (PRBS), comprising:

receiving the PRBS;

predicting a next bit of the PRBS based on a received portion of the PRBS;

comparing the received next bit with the predicted next bit to detect if there is an error in the received next bit; and

upon detecting the error, correcting the received next bit in the PRBS.

15. A method as claimed in claim 14, further comprising:

predicting another next bit of the PRBS based on a portion of the PRBS including the corrected received next bit.

16. A method as claimed in claim 14, wherein the step of correcting the received next bit comprises changing the value of the received next bit.

17. A method as claimed in claim 14, wherein the step of correcting the received next bit comprises correcting the error in the received next bit during the predicting step.

18. A method as claimed in claim 14, wherein the step of predicting a next bit of the PRBS based on a received portion of the PRBS comprises storing the received portion of the PRBS in a linear series of shift registers, and tapping the output of two of the shift registers.

19. A method as claimed in claim 18, wherein the tapping step comprises tapping the output of the last shift register.

20. A method as claimed in claim 18, wherein predicting step further comprises performing an exclusive OR operation on the tapped output of the two shift registers to output the predicted next bit.

21. A method as claimed in claim 18, wherein the step of correcting the received next bit comprises correcting the received next bit as it propagates through the shift registers.

22. A method as claimed in claim 18, wherein the step of correcting the received next bit comprises correcting the received next bit as the received next bit propagates from an output of a first shift register to an input of a second consecutive shift register.

23. A method as claimed in claim 14, wherein the comparing step comprises generating an output signal indicative of an error in the received next bit.

24. A method as claimed in claim 23, further comprising the steps of monitoring the output signal over a predetermined period, and switching on the correcting step when the output signal indicates no error during the predetermined period.

25. A method as claimed in claim 23, wherein the correcting step comprises receiving the output signal indicative of an error in the received next bit.

26. A method as claimed in claim 14, wherein the comparing step comprises detecting a difference between the predicted next bit and the received next bit to detect if there is an error in the received next bit.

27. A method as claimed in claim 26, wherein the step of detecting a difference between the predicted next bit and the received next bit comprises performing an exclusive OR operation on the received next bit and the predicted next bit.

28. A method of detecting error bits in a pseudo-random bit sequence, comprising:

predicting a next bit of the pseudo-random bit sequence based on a stored portion of the pseudo-random bit sequence;

comparing a received next bit of the pseudo-random bit sequence with the predicted next bit to detect an error in the received next bit;

storing the received next bit for future predicting steps; and

upon detecting an error in the received next bit, correcting the value of the stored received next bit to prevent erroneous future predicting steps.

29. A method of detecting error bits in a pseudo-random bit sequence, comprising:

a) receiving a portion of a pseudo-random bit sequence;

b) predicting a subsequent bit of the pseudo-random bit sequence based on the received portion of the pseudo-random bit sequence;

c) receiving a subsequent bit of the pseudo-random bit sequence;

d) comparing the received subsequent bit with the predicted subsequent bit to detect if the received subsequent bit is an error bit;

e) repeating steps b) to d) for subsequently received bits of the pseudo-random bit sequence; and

f) upon detection of an error bit, changing the value of the error bit in the received portion of the pseudo-random bit sequence to prevent incorrect prediction of subsequent bits in step b).

30. A method of detecting errors in a pseudo-random bit sequence, comprising:

receiving a pseudo-random bit sequence into a pseudo-random bit sequence generator to predict a subsequent bit in the pseudo-random bit sequence,

comparing a subsequently received bit of the pseudo-random bit sequence with the predicted bit to generate an error signal indicative of error bits in the pseudo-random bit sequence, and

correcting the value of error bits received in the pseudo-random bit sequence generator to prevent erroneous prediction of further errors.

31. A method of detecting error bits in a pseudo-random bit sequence, comprising:

a) receiving a portion of a pseudo-random bit sequence;

b) predicting the next bit in the pseudo-random bit sequence based on the received portion;

c) receiving the next bit in the pseudo-random bit sequence;

d) comparing the received next bit of the pseudo-random bit with the predicted next bit to detect if the received next bit is an error bit in the pseudo-random bit sequence;

e) repeating steps b) to d) for subsequently received bits of the pseudo-random bit sequence; and

f) changing the value of the error bit in the received portion of the pseudo-random bit sequence to prevent incorrect prediction of the next bit in step b).

32. A method of detecting errors in a pseudo-random bit sequence (PRBS) having a pattern count equal to 2^N – 1, comprising:

receiving N sequential bits of the PRBS into an N-state shift register,

tapping the N-state shift register to generate an predicted next bit of the PRBS,

receiving a next bit of the PRBS into the N-state shift register,

comparing the received next bit with the predicted next bit to generate an error signal, and

in response to the error signal, injecting a correction signal into the N-state shift register to change the value of the received next bit in the N-state shift register.

ABSTRACT

Error Detector With Correction Circuit

An error detector comprising a correction circuit which is a responsive to the output signal indicating an error in the received next bit for correcting the error in the received next bit. The detector may also comprises a predictor configured to receive a portion of the PRBS and predict a next bit of the PRBS based on the received portion, and a comparator configured to receive the next bit of the PRBS, compare the received next bit with the predicted next bit to detect if there is an error in the received next bit, and output a signal indicative of an error in the received next bit.

[Figure 4]

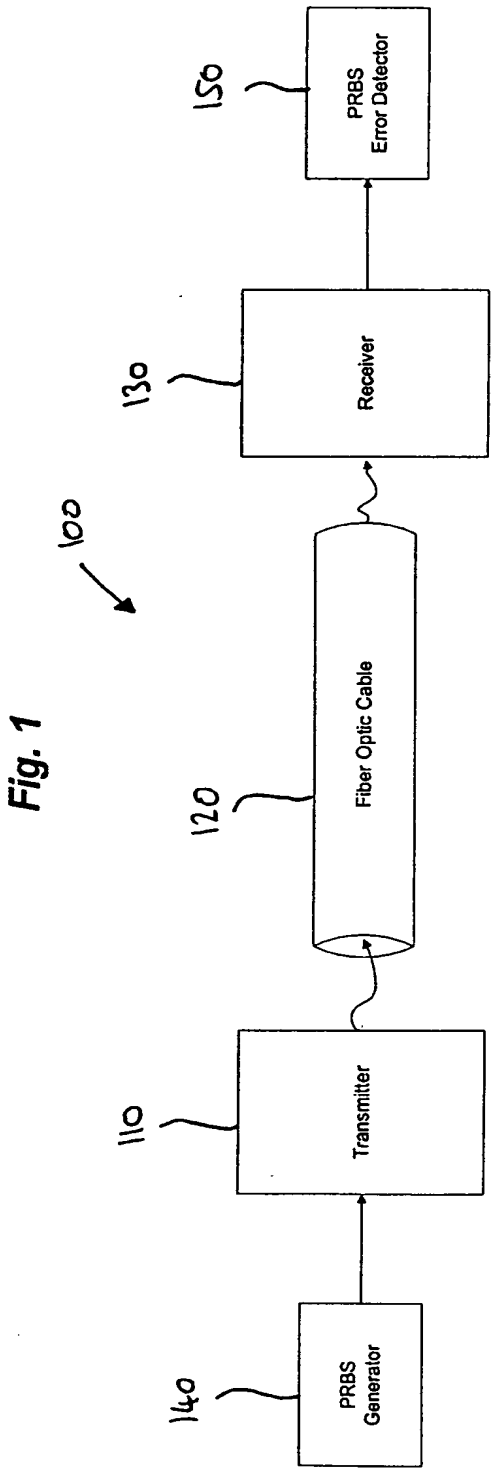

100
110
Transmitter
120
Fiber Optic Cable
130
Receiver
140
PRBS Generator
150
PRBS Error Detector

Fig. 1

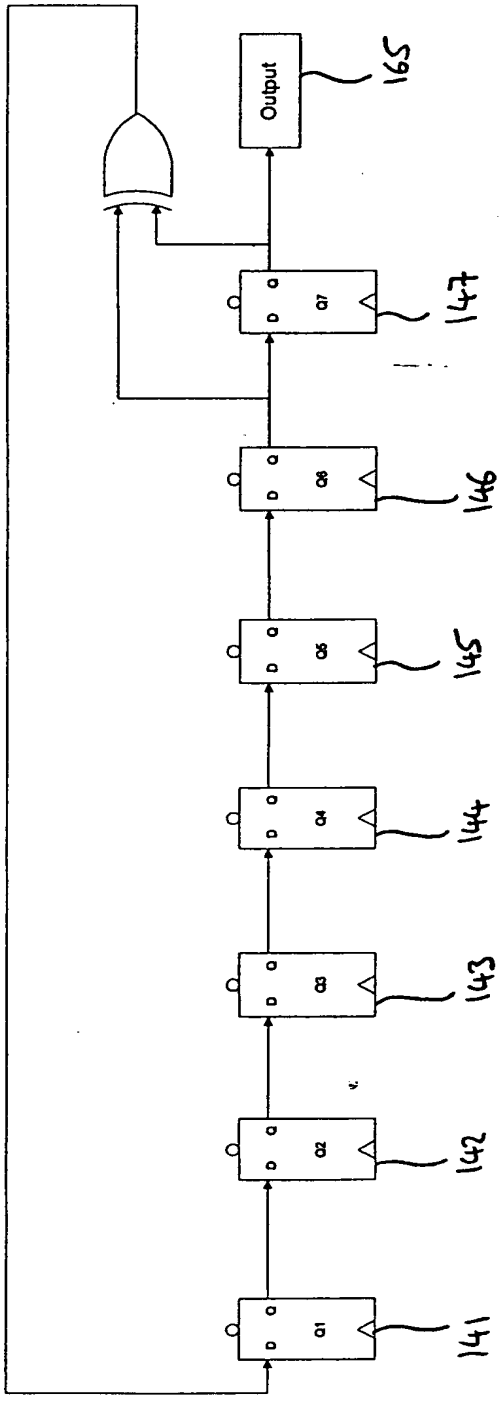


Fig. 2

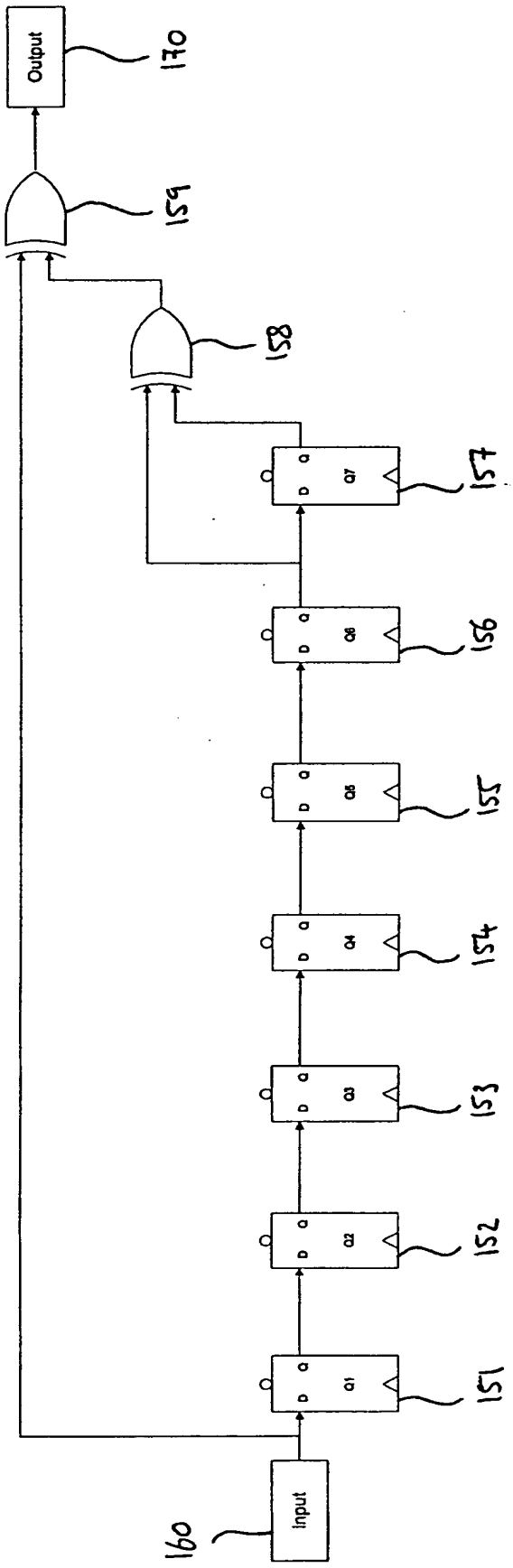

Output
170
159
158
Q7
157
Q6
156
Q5
155
Q4
154
Q3
153
Q2
152
Q1
151
Input
160

Fig. 3

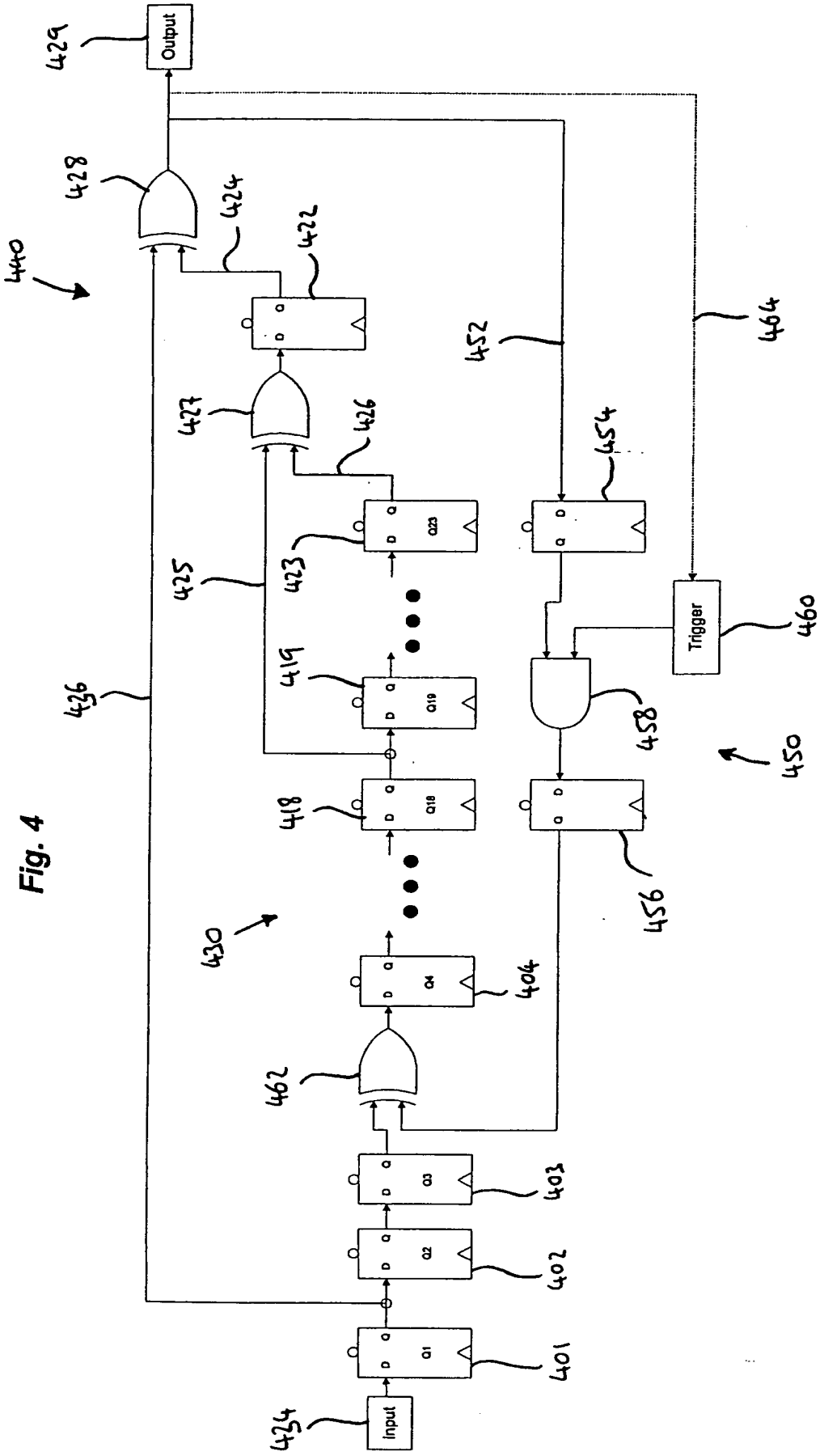

Output
Input
Trigger
Q1
Q2
Q3
Q4
Q18
Q19
Q23
401
402
403
404
418
419
423
424
425
426
427
428
429
430
436
440
450
452
454
456
458
460
462
464

Fig. 4

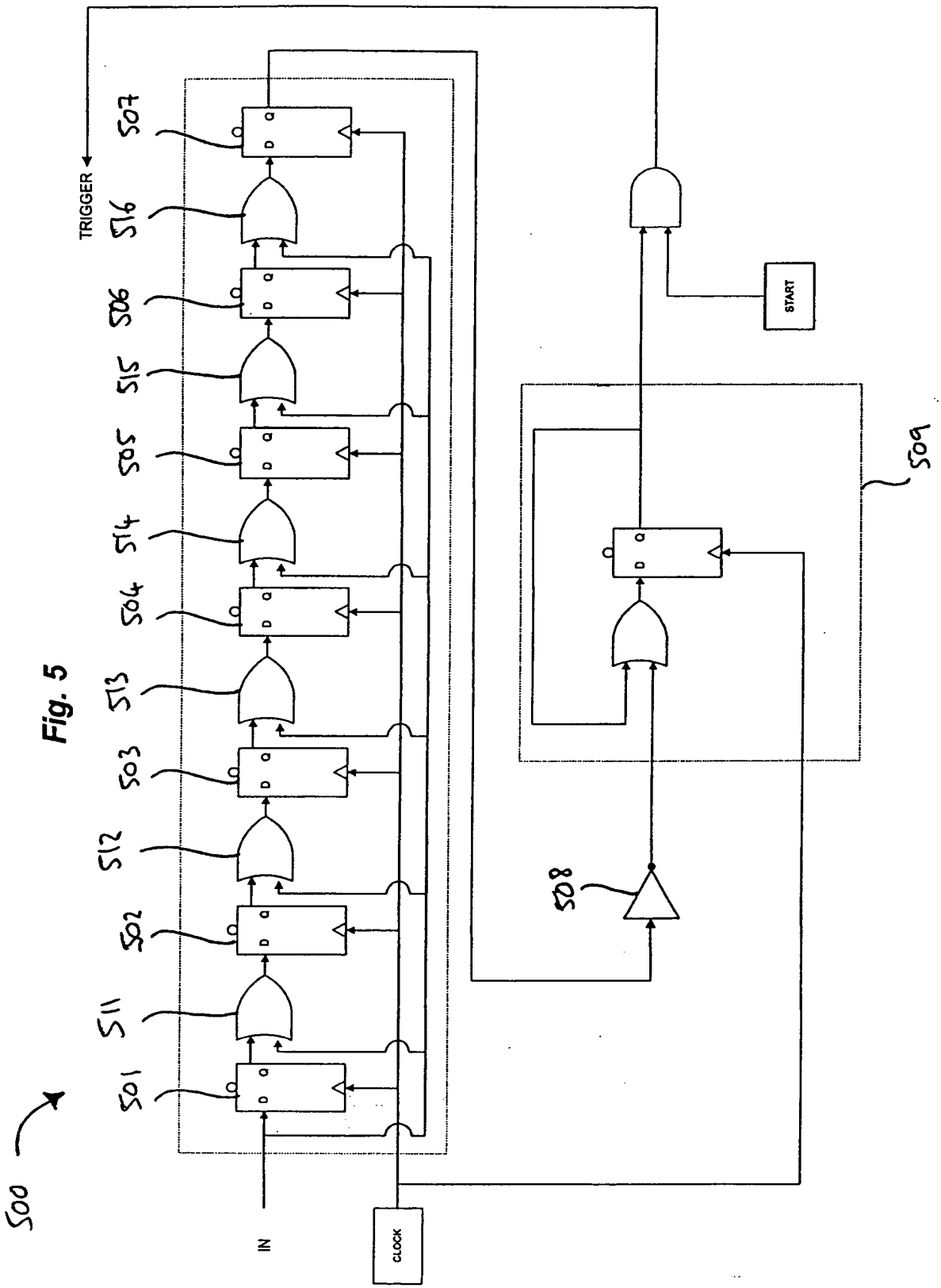

TRIGGER
START
CLOCK
IN
500
501
502
503
504
505
506
507
508
509
511
512
513
514
515
516

Fig. 5

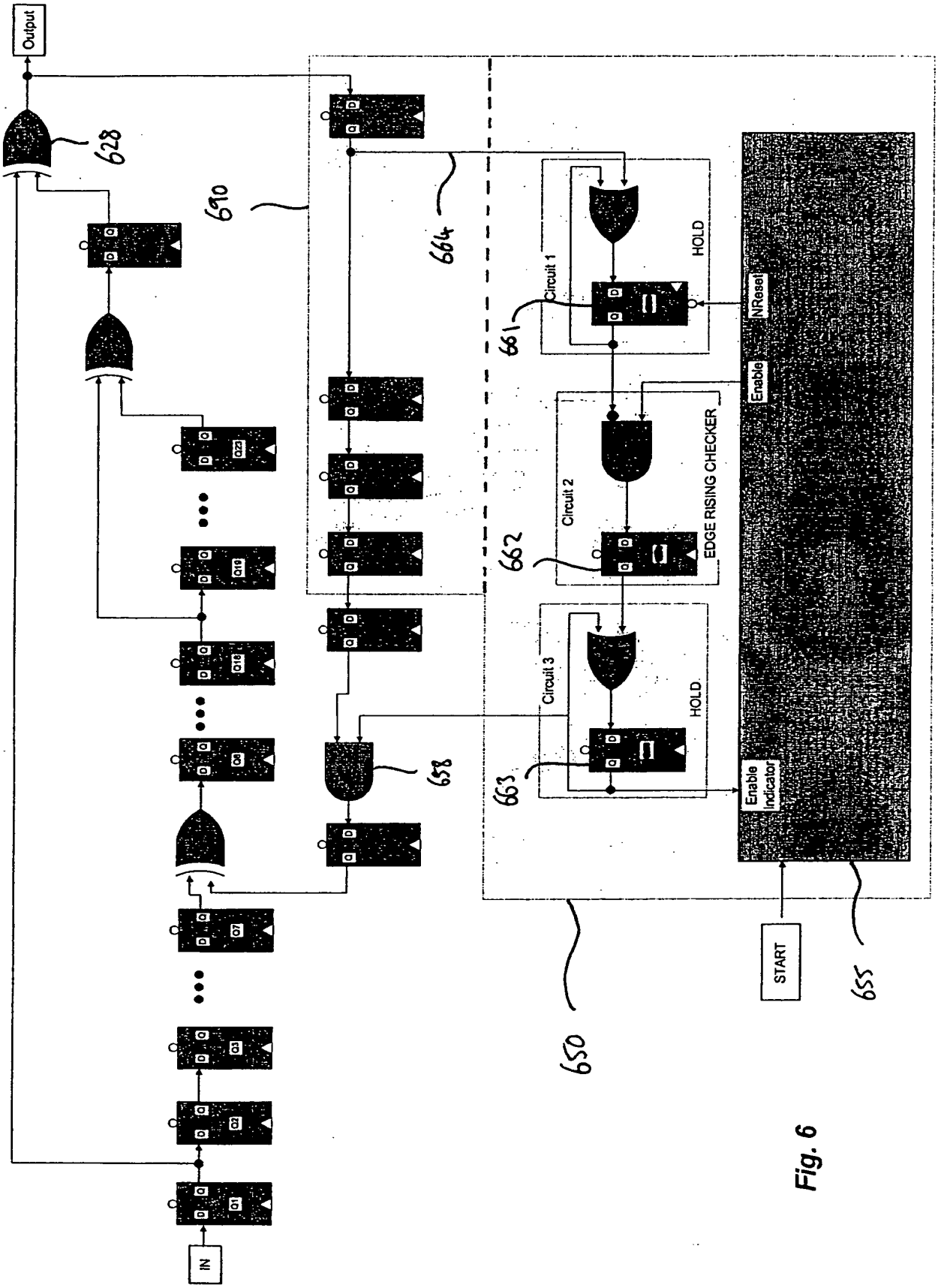

Output
628
690
664
IN
Circuit 1
HOLD
661
NReset
Enable
Circuit 2
EDGE RISING CHECKER
662
Circuit 3
HOLD
663
Enable Indicator
658
START
650
655

Fig. 6

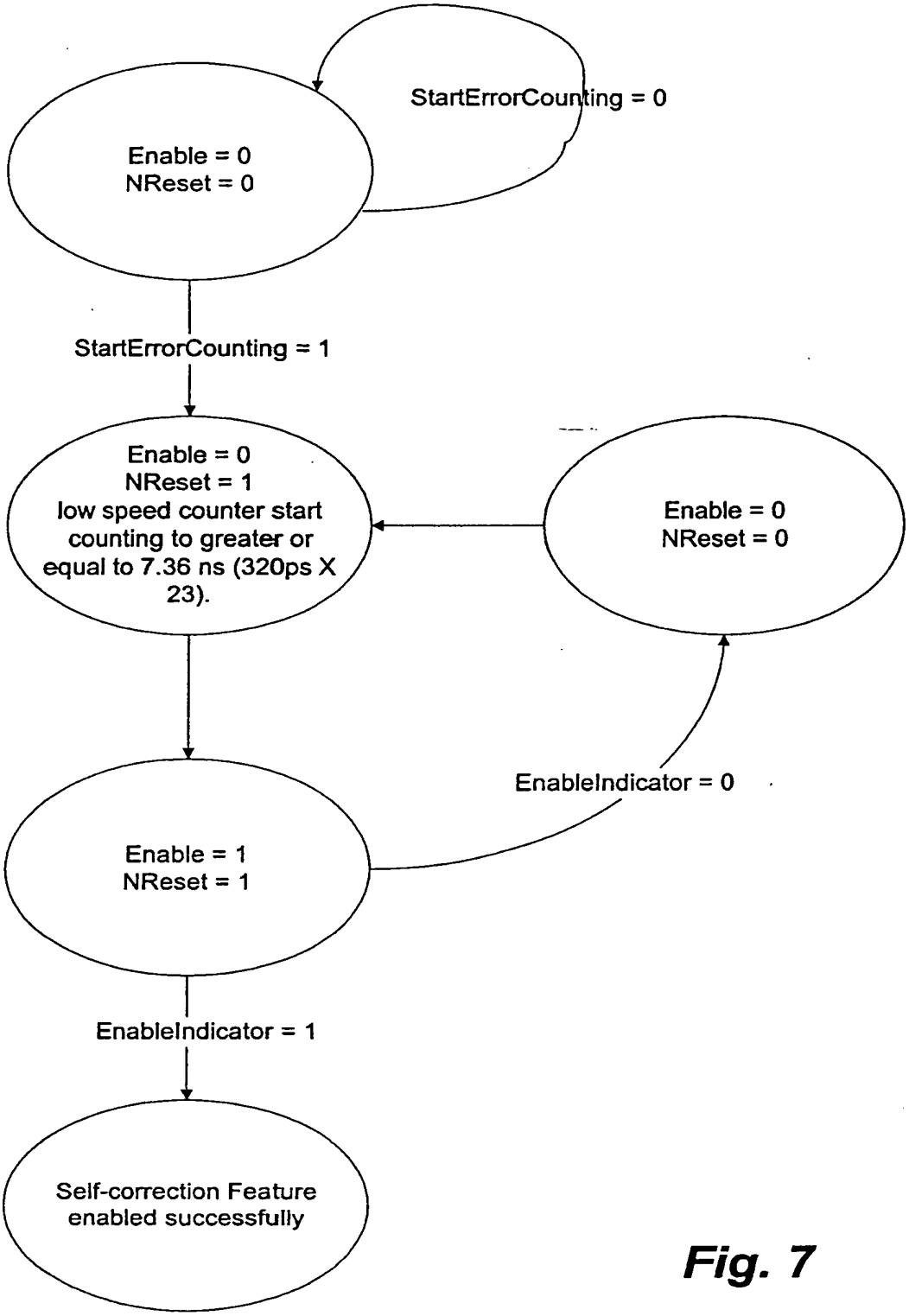

StartErrorCounting = 0
Enable = 0
NReset = 0
StartErrorCounting = 1
Enable = 0
NReset = 1
low speed counter start counting to greater or equal to 7.36 ns (320ps X 23).
Enable = 0
NReset = 0
EnableIndicator = 0
Enable = 1
NReset = 1
EnableIndicator = 1
Self-correction Feature enabled successfully

Fig. 7

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